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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/713,879

11/13/2003

Ansheng Liu

42P17910

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7590

11/02/2005

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EXAMINER

CHIEM, DINH D

ART UNIT

PAPER NUMBER

2883

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

24

Office Action Summary	Application No. 10/713,879	Applicant(s) LIU ET AL.	
	Examiner Erin D. Chiem	Art Unit 2883	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 August 2005.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-27 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This office action is in response to Applicant's amendment filed on August 22, 2005.

Currently claims 1-27 are pending.

Drawings

The objections made in the office action with the mailing date May 19, 2005 are withdrawn in view of the replacement drawings.

Claim Objections

The objection to claim 22 is withdrawn in view of the amended limitation –*optical beam*–.

Claim Rejections - 35 USC § 112

The rejection to claims 6, 10, 11, 16, 17, and 26 are withdrawn in view of the amended limitation –*lateral taper*–.

However the rejection for claims 7, 18, 19, and 27 is maintained since the Specification lacks support of the –*fourth lateral taper rate*–. Figure 5 shows 3 tapering rates and as followed:

- First rate: $W_0 \rightarrow W_1$
- Second rate: $W_0 \rightarrow W_2$
- Third rate: $W_0 \rightarrow W_3$
- Fourth rate: ??

(Note: the rate numbering is arbitrary)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-13 and 14-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeon et al. (US Patent 6,174,748 B1, Jeon hereinafter) in view of Yamamoto et al. (US 6,030,540, Yamamoto hereinafter).

Regarding claims 1, and 8-13 Jeon teaches an apparatus comprising a buried tapered waveguide, referring to Fig. 2, reference number 14A, disposed in a semiconductor layer 10, and a tapered rib waveguide disposed in a semiconductor layer 29, the tapered rib waveguide including a rib portion adjoining a slab portion 16A, the slab portion of the rib waveguide adjoining the buried tapered waveguide. As to the direction of the input light, Jeon teaches the apparatus is bidirectional wherein the coupling of input light is dependent on whether the user wishes to transform a large mode to a single mode or vice versa. Different mode coupling is performed by the tapering region wherein the light traveled through the larger or smaller end of the mode converter, when the light reaches the tapering region the two different modes are coupled together and then passed on through to either a larger mode or a smaller mode (col.1, line 49-61). With regard to the lateral tapering of the rib waveguide, please the lateral tapering progression of elements 16A and 14A in Fig. 2.

Regarding claims 2-5, the first and second cladding layers are a part of the semiconductor substrates made of indium phosphide layers (col. 3, line 22-27) wherein cladding layers are laterally grown onto the semiconductor substrate for the purpose of confining lights within the active light guiding layers. The buried tapered waveguide is also insulated within the cladding layers. See Fig. 2 for further details.

Regarding claim 6 and 7, the rejection made to the limitation of the *fourth taper rate*—is reasserted herein and will not be given patentable weight. In Figure 2, Jeon clearly shows two different taper rates. Applicant further explains that the “specific dimensions and taper rates illustrated herewith are provided for explanation purposes and that other dimensions or rates may also be utilized in accordance with the teachings of the present invention.” Thus, it would have been obvious to one of ordinary skill in the art, such as Jeon, further etch the rib waveguide to a sharp point equating to Applicant’s third taper rate since the taper rate reduces or increases the mode field of the smaller end of the waveguide. And one of ordinary skill in the art would understand the various taper rates allow mode field conversion of various waveguide mode field sizes.

Regarding claims 14-21, Jeon also anticipates the method of making a dual tapered waveguide. The etching process begins with etching on a semiconductor wafer (Fig. 3A) through the first mask 31 and the etching of the buried taper waveguide is via a second mask 32 having a larger width end 36 and a smaller width end 34; growing an insulating layer about 100nm to 200 nm thick of SiO₂. The etching process is then patterned the tapered rib waveguide in the silicon grown over the buried tapered waveguide such that a slab portion of the tapered rib

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waveguide adjoins the buried tapered waveguide having a larger end and a smaller end (Abstract and (col. 7, line 55 – col. 8, line 13)).

However, Jeon does not explicitly teach the “vertical height of the buried tapered waveguide at the larger end and at a smaller end opposite the larger end are substantially similar.”

In teaching the method for producing tapered waveguide, Yamamoto demonstrated the improvement of his invention over the prior art (Figure 5A-5I). Yamamoto showed that by removing the mask 53 at a predetermine rate, a vertical tapering is formed versus the prior art that maintain the mask 53 such that there is no vertical tapering. Yamamoto’s purpose for forming the vertical tapering is to further narrow the mode field on one end of the waveguide. However, when the vertical element of the mode field is not required to be converted then one of ordinary skill may retain the mask 53 and maintain a substantial similar height for the buried waveguide.

Since Jeon and Yamamoto are from the same field of endeavor, the purpose disclosed by Yamamoto would have been recognized in the pertinent art of Jeon.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to maintain or remove the mask 53, as taught by Yamamoto. **The motivation** for removing the mask 53 is to keep the height at the substantially same height when the vertical element of the mode field is not critical or the mode field conversion requirement is not as stringent.

Claim Rejections - 35 USC § 103

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1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 22-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeon in view of Yamamoto and Soljagic et al. (US 2003/0031443 A1).

Jeon et al. teach a mode converter comprising a semiconductor substrate having dual tapered waveguides wherein there are regions of tapering having different tapering rates such that multi mode signal can be converted to single mode signal and vice versa.

However, Jeon does not explicitly the vertical height of the buried waveguide is substantially the same nor does Jeon teach a system having an optical transmitter to transmit and optical beam and an optical receiver, nor does Jeon et al. explicitly disclose a photonic device optically coupled to the smaller end of the taper rib waveguide from the transmitter by the optical signal to be directed from the tapered rib waveguide through the photonic device to the optical receiver.

In teaching the method for producing tapered waveguide, Yamamoto demonstrated the improvement of his invention over the prior art (Figure 5A-5I). Yamamoto showed that by removing the mask 53 at a predetermine rate, a vertical tapering is formed versus the prior art that maintain the mask 53 such that there is no vertical tapering. Yamamoto's purpose for forming the vertical tapering is to further narrow the mode field on one end of the waveguide. However, when the vertical element of the mode field is not required to be converted then one of

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ordinary skill may retain the mask 53 and maintain a substantial similar height for the buried waveguide.

Soljacic et al. teach coupling the tapered waveguide as a mode size converter to any optical devices such as a photonic integrated circuit (Fig. 21). Soljacic et al. further defines the coupling of tapered waveguide and a photonic integrated circuit as a bi-stable device since the efficiency confine the signal mode by converting a large mode field to a smaller mode field or vice versa enhances the axial confinement and the radial confinement of the optical signal, thereby, one can form optical cavities having high Q values and/or small modal volumes in the waveguides [0013]. Soljacic et al. further applied the bi-stable device as being applicable as an optical regenerator wherein the optical receiver sends its electrical output into an optical transmitter and the transmitter then relay a new optical signal into the fiber. Optical regenerator are used in long-haul transmission applications to remove unwanted effects such as dispersion, nonlinearities, and noise or any other effects that could corrupt the optical signal. When applying the bi-stable device into the optical regenerator, Soljacic et al. demonstrated the all optical signal output from the optical regenerator having definitively two states, high and low (Fig. 42).

Since Jeon, Yamamoto, and Soljacic et al. are from all from the same field of endeavor, the purpose disclosed by Yamamoto and Soljacic et al. would have been recognized in the pertinent art of Jeon.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to provide a mean to control mode field conversion. By removing the mask, the mode field size may further be reduced in the vertical dimension or one of ordinary

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skill may choose to maintain the mask and substantially keep the same height for the buried waveguide when the conversion requirement is not as stringent. Also, it would have been obvious to replace the tapered waveguide used by Soljacic et al. with a dual tapered waveguide taught by Jeon et al. to increase the coupling capability of various optical devices since a dual tapered waveguide may couple an input having any mode field size to one end and efficiently converting the mode such that coupling to the photonic integrated circuit is possible.

Furthermore, one of ordinary skill in the art would know how to apply a taper waveguide as taught by Jeon or Yamamoto in an integrated system. The motivation for coupling the taper waveguide in an integrated system would have been for increasing the flexibility of optical elements that may be coupled to the bi-stable device needed in the long-haul transmission taught by Soljacic et al., since coupling different mode fields is made possible by the bi-stable device, such that an all-optical output will definitively output only two states, high and low, that makes the transmission truly digital.

Response to Arguments

Applicant's arguments with respect to claims 1-27 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Forrest et al. (US Patent 6483863 B2) integrating the tapered waveguide in an integrated system.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erin D. Chiem whose telephone number is (571) 272-3102. The examiner can normally be reached on Monday - Thursday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank G. Font can be reached on (571) 272-2415. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

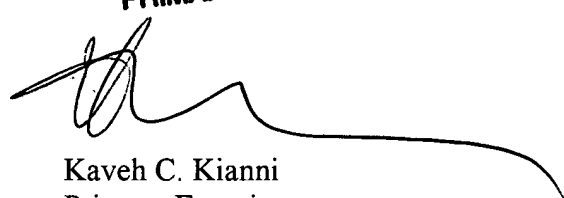
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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Erin D Chiem
Examiner
Art Unit 2883

**KAVEH KIANNI
PRIMARY EXAMINER**



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